CLAIMS

What is claimed:

1. A method for fabricating a capacitor in an interlayer dielectric (ILD) comprising:

forming a via and overlying trench in the ILD;

depositing a first conductive barrier layer so as to line the via and trench;

depositing a dielectric layer over the first conductive barrier layer;

depositing a second conductive barrier layer over the dielectric layer;

filling the via and trench with a conductive material that includes copper over the second conductive barrier layer; and

polishing back the conductive material so as to expose the ILD adjacent to the trench.

2. The method defined by claim 1 wherein the barrier layer comprises tantalum.

3. The method defined by claim 1 wherein the dielectric layer is selected from the group consisting of silicon nitride, titanium oxide, tantalum penta oxide, or barium-strontium-titanate.

4. The method defined by claim 1 including the deposition of a conductive electrode layer between the first conductive barrier layer and the dielectric layer and between the dielectric layer and the second conductive barrier layer.

5. The method defined by claim 4 wherein the electrode layers comprise a material selected from the group of ruthenium or iridium.

6. The method defined by claim 1 wherein the via exposes an underlying conductor.

7. The method defined by claim 1 wherein a plurality of vias and trenches are simultaneously formed in the ILD and where prior to the filling of the vias and trenches, selected vias and trenches are masked and the remaining vias and trenches are etched to remove the second conductive barrier layer and the dielectric layer.

8. The method defined by claim 7 wherein the barrier layer comprises tantalum.

9. The method defined by claim 7 wherein the dielectric layer is selected from the group consisting of silicon nitride, titanium oxide, tantalum penta oxide, or barium-strontium-titanate.

10. The method defined by claim 1 including the deposition of a conductive electrode layer disposed between the first conductive barrier layer and the dielectric layer and between the dielectric layer and the second conductive barrier layer.

11. The method defined by claim 10 wherein the electrode layers comprise a material selected from the group of ruthenium or iridium.

12. The method defined by claim 1 wherein the via exposes an underlying conductor.

13. In a dual damascene process an improvement comprising:

lining selective vias and trenches with a first and second barrier layer having a dielectric disposed therebetween prior to a copper layer formation; and

polishing the copper layer.

14. The process defined by claim 13 wherein the dielectric is selected from the group consisting of silicon nitride, titanium oxide, or barium-strontium-titanate.

15. The process defined by claim 13 wherein the conductive barrier layer comprises tantalum

16. The process defined by claim 13 wherein electrode layers are used between the barrier layers and the copper layer.

17. The process defined by claim 13 where the first barrier layer is in contact with an underlying conductor.

18. A method for fabricating capacitors and via interconnects in an interlayer dielectric (ILD) comprising:

forming vias and overlying trenches;

forming a capacitor structure on the ILD and within the vias and trenches;

removing a dielectric layer from the capacitor structure from selected vias and trenches.

19. The method defined by claim 18 including the steps of forming a copper layer and polishing the copper layer after the step of removing the dielectric from the capacitor structures in selected vias and trenches.

20. The method defined by claim 19 wherein the polishing step includes removing all material on the ILD between the trenches.

21. The method defined by claim 19 wherein the step of forming the capacitor structure comprises the steps of forming a first conductive barrier layer, forming a dielectric and forming a second conductive barrier layer.

22. The method defined by 21 including the steps of adding electrode layers between the barrier layers and the dielectric.

23. A capacitor comprising a first and second conductive layer separated by a dielectric defining a first stepped sidewall, a mirror image second stepped sidewall facing the first sidewall and a base disposed between the lower ends of the first and second sidewalls.

24. The capacitor defined by claim 23 wherein the first and second conductive layers comprise a metal which acts as a barrier layer to copper.

25. The method defined by claim 24 including additional metal layers disposed between the first conductive layer and the dielectric and the second conductive layer and the dielectric.

26. The capacitor defined by claim 23 wherein the dielectric is selected from the group consisting of silicon nitride, titanium oxide, tantalum penta oxide, or barium-strontium-titanate.